

<b>Notice of References Cited</b>	Application/Control No. 10/711,838	Applicant(s)/Patent Under Reexamination CHOU, PEI-YU	
	Examiner Eric B. Chen	Art Unit 1765	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,692,903	02-2004	Chen et al.	430/329
	B	US-2003/0228532	12-2003	Mui et al.	430/30
	C	US-5,882,489	03-1999	Bersin et al.	204/192.35
	D	US-6,322,714	11-2001	Nallan et al.	216/67
	E	US-6,440,864	08-2002	Kropewnicki et al.	438/710
	F	US-6,541,843	04-2003	Yin et al.	257/639
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	K	US-			
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	M	US-			

**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, Silicon Processing for the VLSI Era, 2002, Lattice Press, Vol. 4, p. 248.
	V	Wolf et al., Silicon Processing for the VLSI Era, 1986, Lattice Press, Vol. 1, p. 523.
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	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.